



# GOVERNMENT COLLEGE OF ENGINEERING, JALGAON

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Name of Examination : **Winter 2020** - (Preview)

Course Code & Course Name : **ET401 - Digital System Design and Very Large Scale Integra**

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Maximum Marks : **60**

Duration : **3 Hrs**

[Edit](#) [Print](#) [View Answer Key](#) [Close](#) **Answer Key Submission Type:** Marking scheme with model answers and solutions of numerical

Instructions:

1. All questions are compulsory.
2. Illustrate your answer with suitable figures/sketches wherever necessary.
3. Assume suitable additional data; if required.
4. Use of logarithmic table, drawing instruments and non programmable calculators is allowed.
5. Figures to the right indicate full marks.

## 1) Solve any two sub questions.

- A) Explain various operators used in VHDL [6]
- B) If A and B are two unsigned variables with A = **1100** & B = **1001** then find following (i) A **OR** B (ii) A **NOR** B (iii) A **SLR** 3 (iv) B **ROR** 3 (v) A & B (vi) A **AND** B (vii) A **SLL** 1 (viii) A **XNOR** B [6]
- C) Discuss VHDL data types in detail. [6]

## 2) Solve any two sub questions.

- A) Design and write data flow description for 2 bit magnitude comparator  $A_{(1)}A_{(0)}$  and  $B_{(1)}B_{(0)}$  with output  $Y_{\text{greater}}$ ,  $Y_{\text{less}}$  and  $Y_{\text{equal}}$ . Where  $A_{(0)}$  and  $B_{(0)}$  are least significant bits. [6]
- B) Write structural and behavioral description for 1 bit full adder. [6]
- C) Explain constants, signals and variables in VHDL. Give suitable example to illustrate difference between signal and variable. [6]

## 3) Solve any two sub questions.

- A) Compare IF statement and CASE statement with example. [6]
- B) Write VHDL description for SR-Latch using structural style of description. [6]
- C) Explain bindings in VHDL with suitable examples. [6]

## 4) Solve all sub questions.

- A) What is package? Give syntax rule for package with suitable example. [6]
- B) Write VHDL code for addition of two [4 x 4] matrices. [6]

## 5) Solve all sub questions.

- A) Explain with neat diagram architecture of Xilinx Spartan 4000 series FPGA [6]
- B) Draw and Explain architecture of Xilinx 9500 CPLD series. [6]

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